

Brain-like Computing - Technologies and Architectures

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Ann Arbor, MI 48105

**Acknowledgement: National Science
Foundation (CCF & ECCS)**

EVOLUTION OF NEUROMORPHIC COMPUTING:

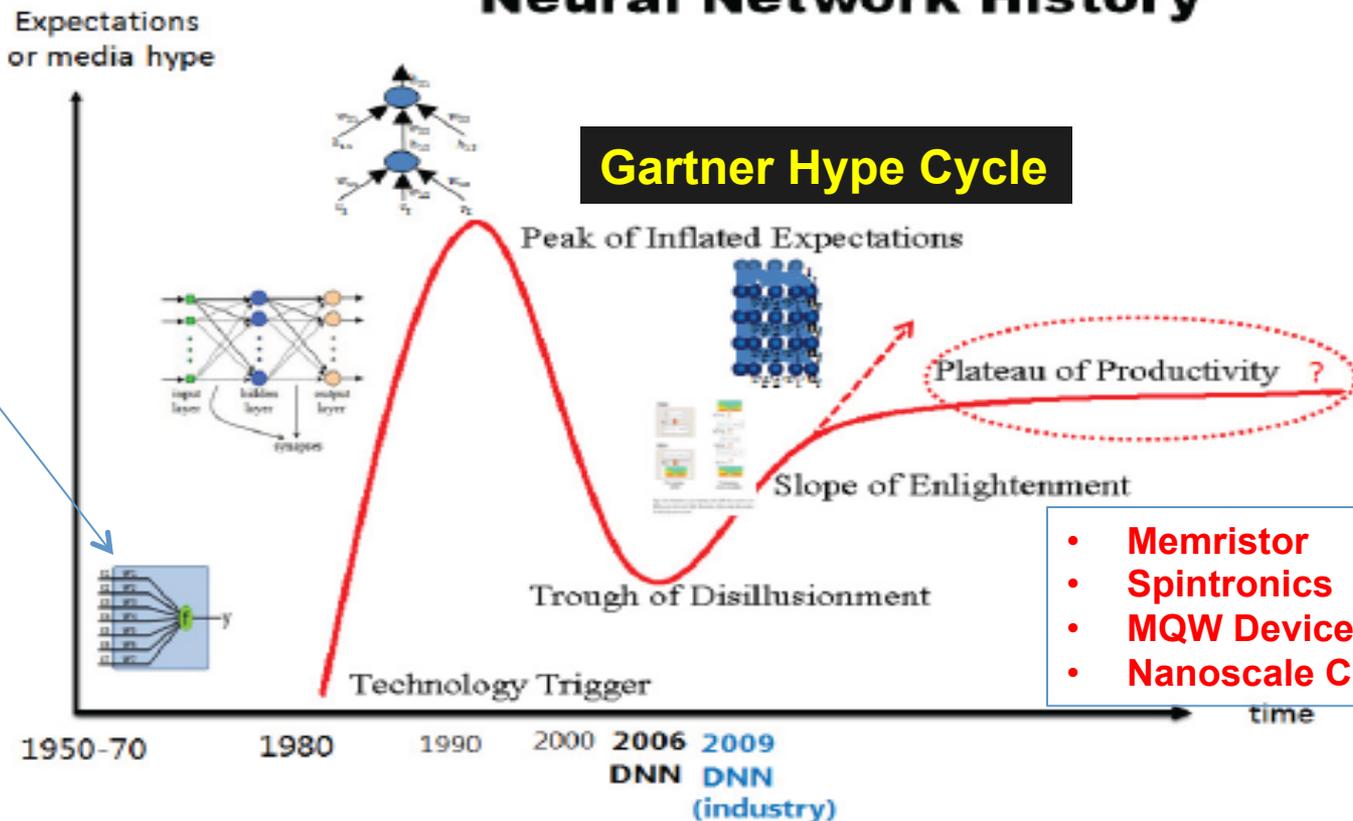
Perceptron ('60)
(10 E 2 neurons)

Neural Net ('90)
(10 E 3 Neurons)

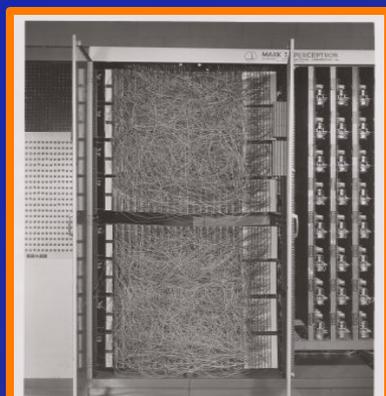
Neuromorphic Hardware ('00)
(10 E 5 neurons)

Multi-level Nanocrossbar
(10 E 7 neurons)

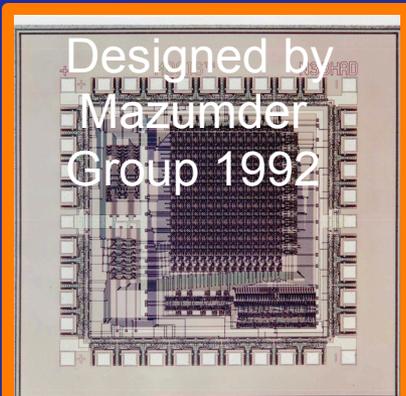
Neural Network History



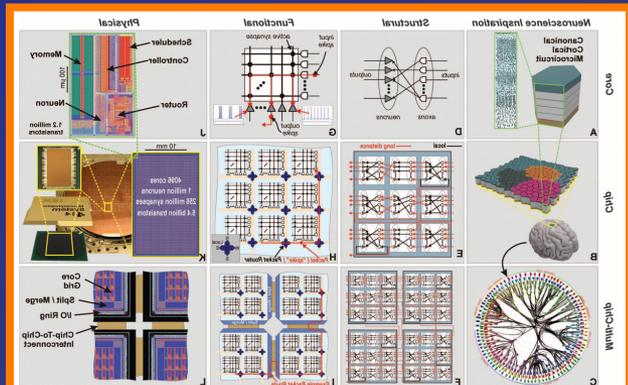
- Memristor
- Spintronics
- MQW Devices
- Nanoscale CMOS



Perceptron Mark 1



Hopfield Net Chip



TrueNorth (IBM) ~ 1 M Neurons

Mazumder Group's Neuromorphic Research

Self-Healing VLSI Design (1989-1996)

Hopfield Neural Net as Algorithmic Hardware for Spare Allocation by Node Cover over Bipartite Graph

- IEEE Trans. on CAS, 1993
- IEEE Trans. on CAS, 1993
- IEEE Trans. on Computer, 1996

Cellular Neural Networks (2008-2013)

- Color Image Processing
- Velocity Tuned Filter
- Memristor/RRAM based CNN
- RTD+HEMT based CNN
- IEEE Trans. on VLSI, 2009
- IEEE Trans. on Nanotechnology, 2008
- IEEE Trans. on Neural Nets, 2014
- IEEE Trans. on Nanotechnology, 2013
- ACM Journal on Emerging Technologies in Computing Systems, 2013

Learning based VLSI Chips (2010-2016)

STDP Learning for Position Detector
STDP Learning for Virtual Bug Navigation
STDP Learning for XOR/Edge Detection

Q-Learning for Maze Search Algorithm on Memristor Array

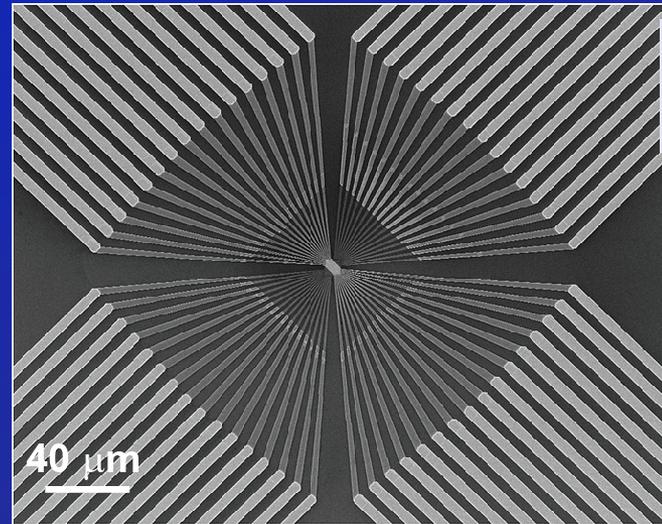
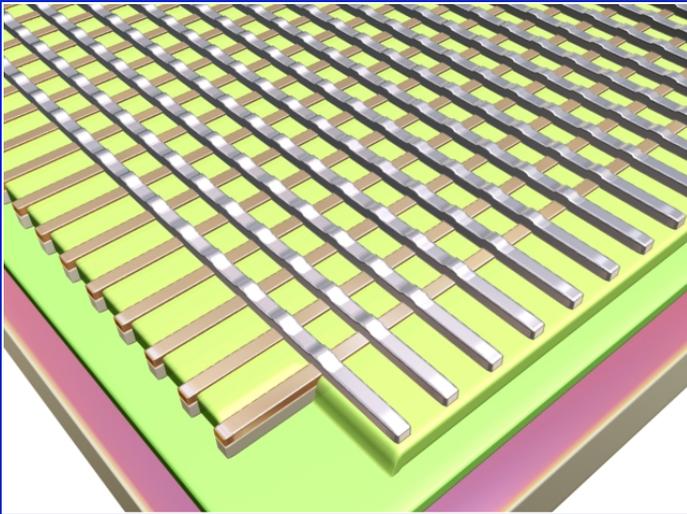
Reinforcement Learning/Actor-Critic NN for Optimal Nonlinear Control Applications

- Proceedings of the IEEE, 2012
- Nano Letters Journal, 2010
- IEEE Trans. on Computer, 2016
- IEEE Nanotechnology, 2011
- IEEE Nanotechnology, 2014
- IEEE Cellular Neural Networks, 2012

Neuromorphic Self-Healing Memory Design using Memristor Array

Product Code (SEC), Augmented PC (DEC) → Requires Muxes (~8%)
Hamming Code (SEC) → Higher Overhead
Projective Geometry Code (DEC/TED) → Galois Field Decoding, ...
BCH & Reed Solomon (DEC) → Decoding complexity is high

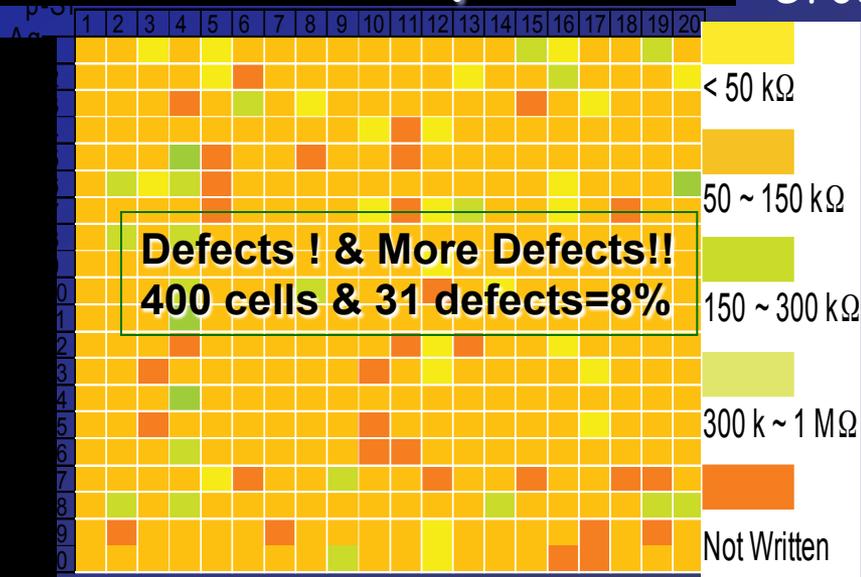
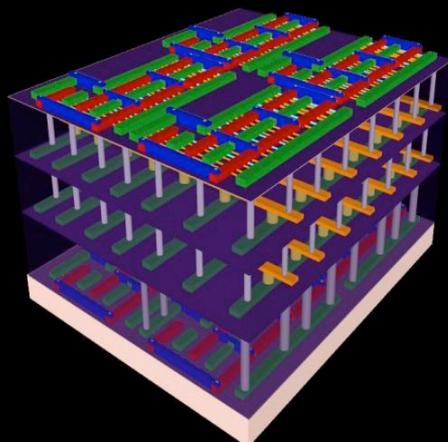
High Density a-Si Based Nano-Crossbar



1 kb crossbar array

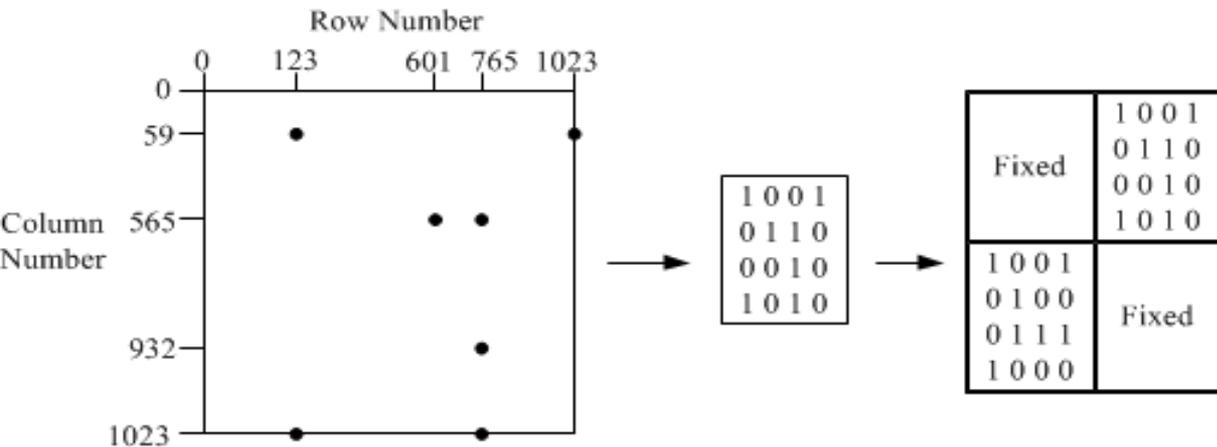
Jo et al.
Nano Lett.,
 9, 870
 (2009).
 From Prof.
 Wei Lu's
 Research
 Group

It is Scalable and CMOS Compatible.



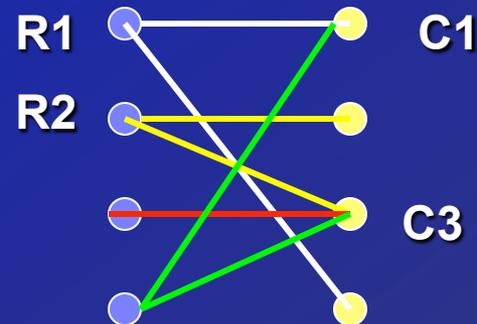
Fabbed by
 Wei Lu's
 Group at
 Univ. of
 Michigan

Compaction of Faulty Array & Find Vertex Cover in Bipartite Graph



Mazumder & Yih, IEEE Trans. on CAD, 1992

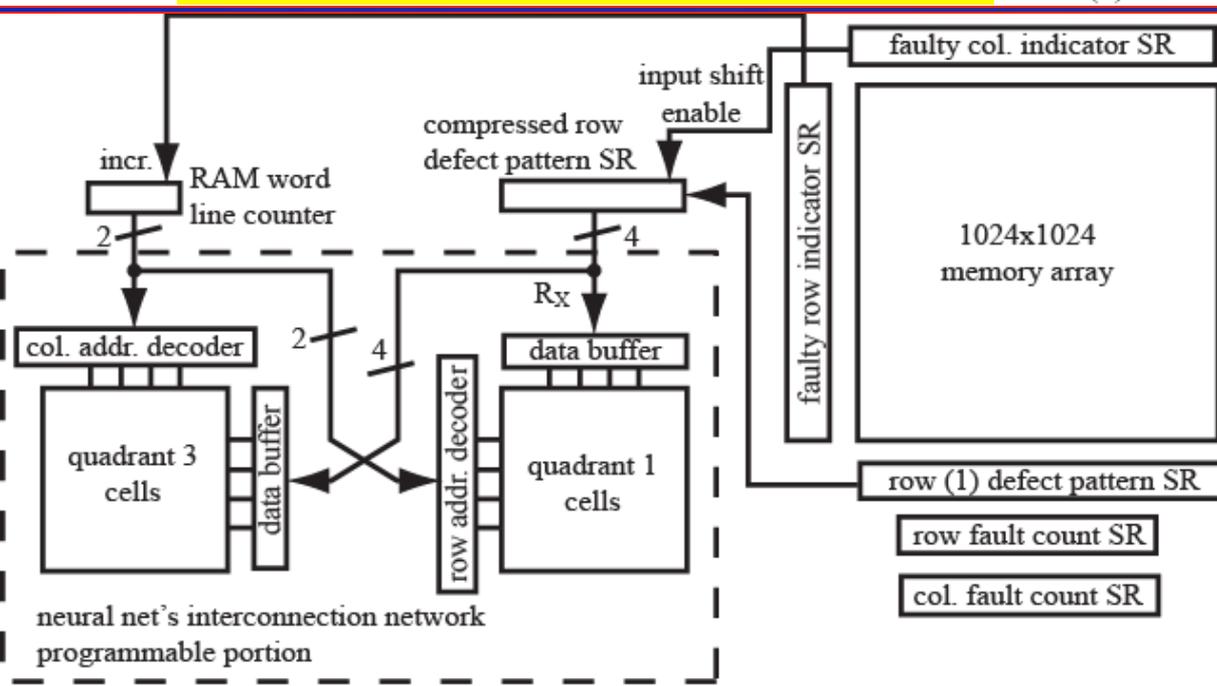
(c)



Find Vertex Cover:

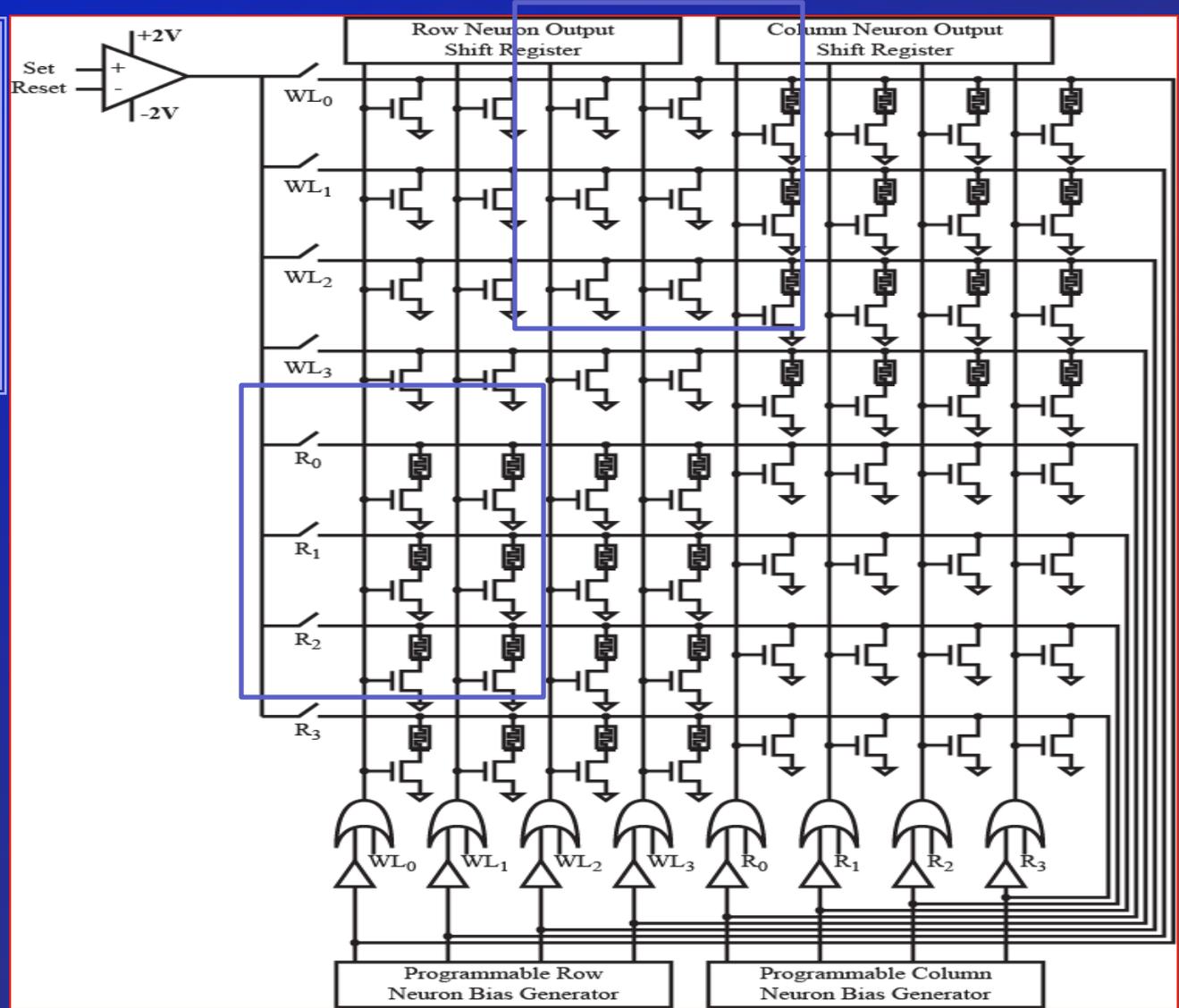
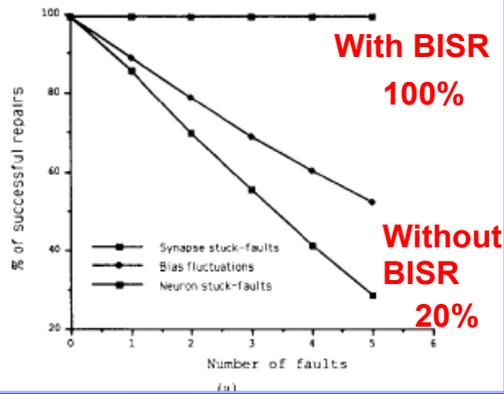
[R1, R2; C1, C3]

Defective Cells are Edges in Bipartite Graph

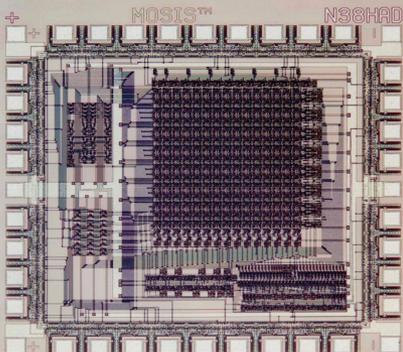


Unrestricted Vertex Cover Problem can Be solved in Polynomial Time by Bipartite Graph Matching Algorithm. However, Restricted Vertex Cover Problem is NP-complete.

Neuromorphic Self-Healing for Any Type of Memory Array



M.D. Smith & P. Mazumder,
IEEE Trans. on Computers,
 Vol. 45, No. 1, Jan. 1996, pp.
 109-115.

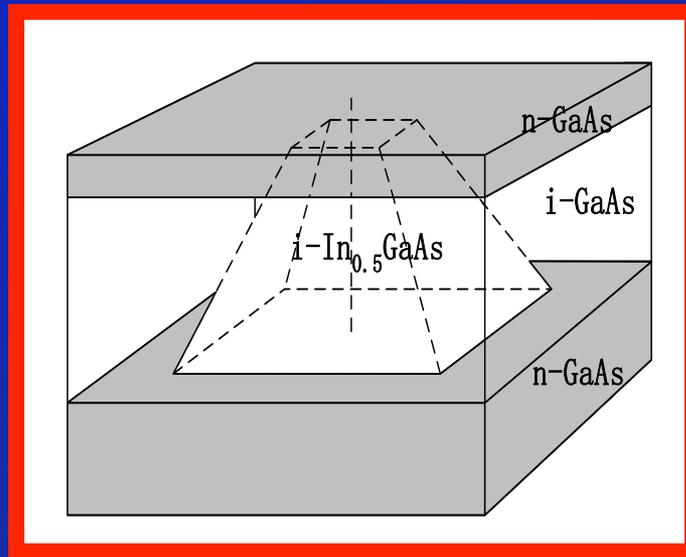
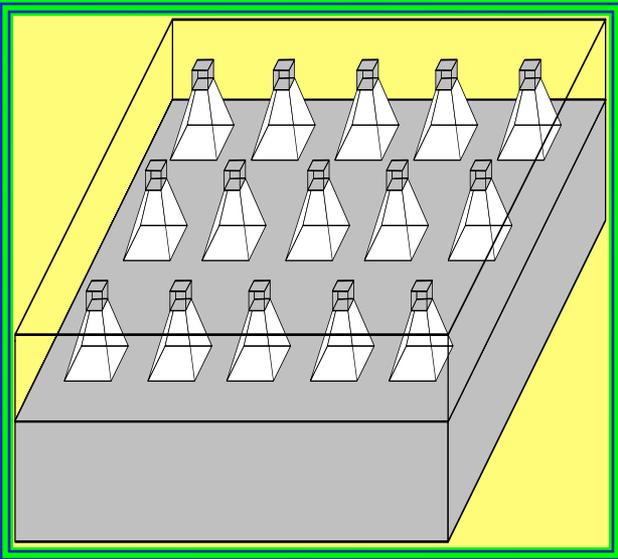


10,000 trans.

Fusion of Sensing & Processing

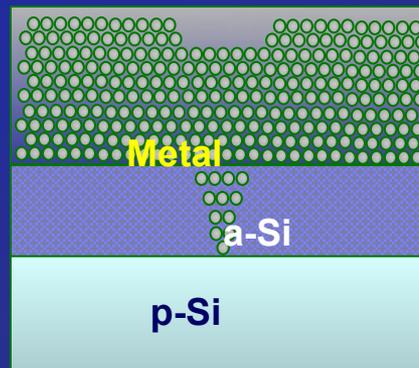
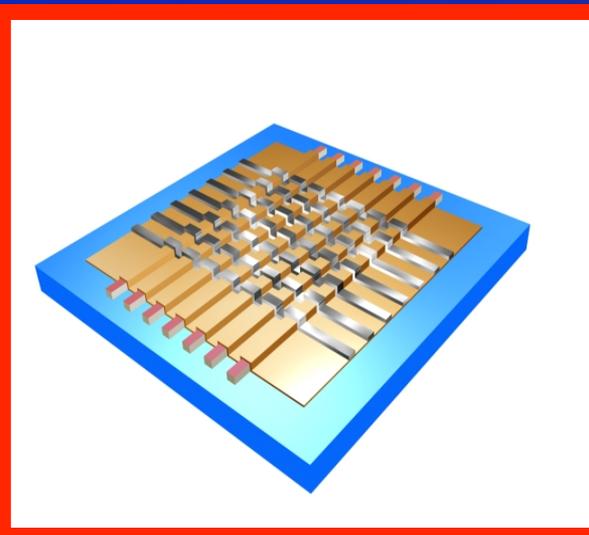
Nanoscale
Cellular Neural Network (CNN)
by Using
Quantum Tunneling Devices &
Memristor Array

Fusion of Sensing & Processing

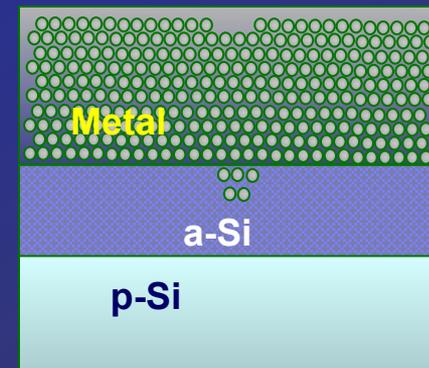


3-D Confined
Quantum Box
Array

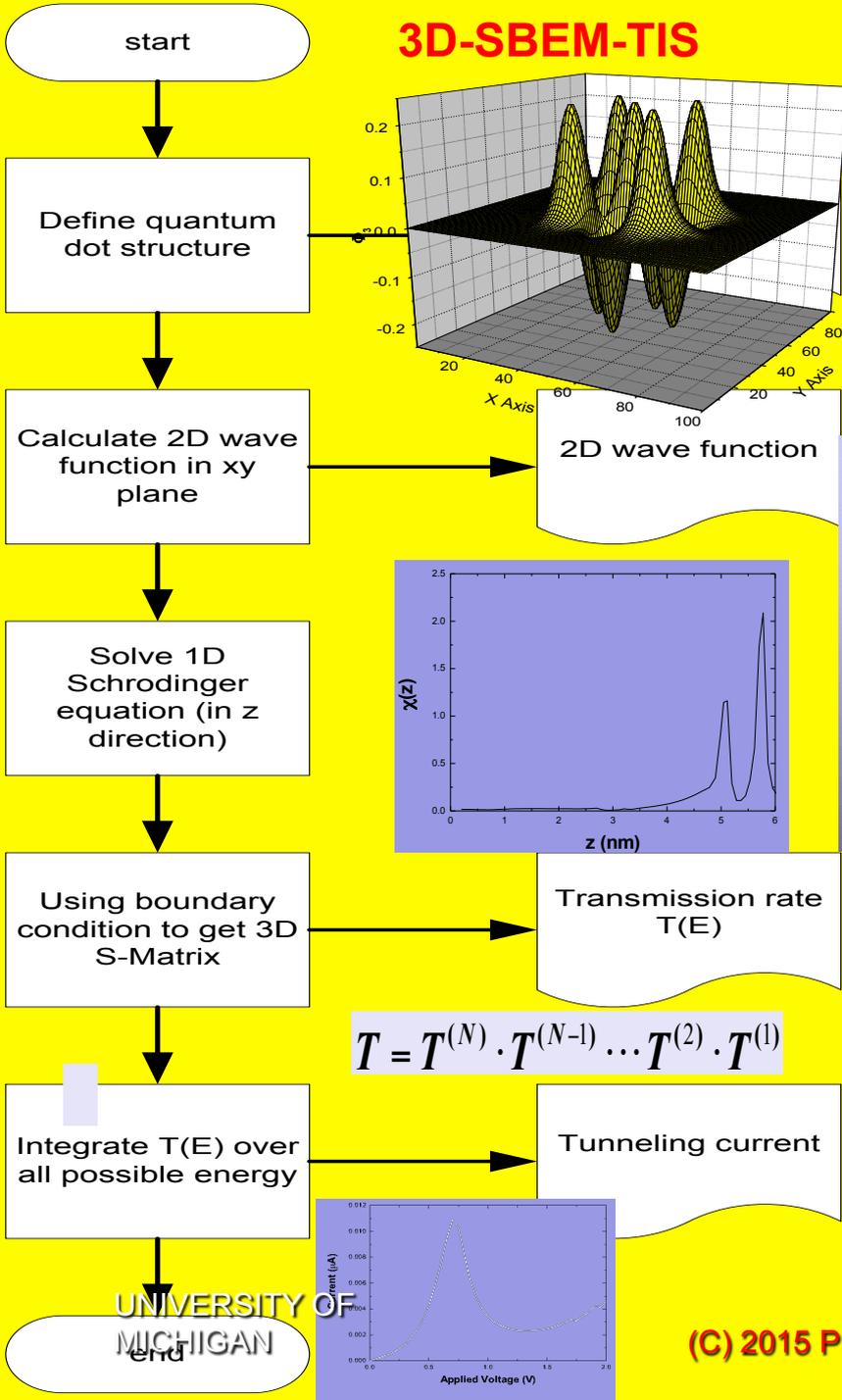
Memristor
Array



Low Resistance
State (LRS)



High Resistance
State (HRS)



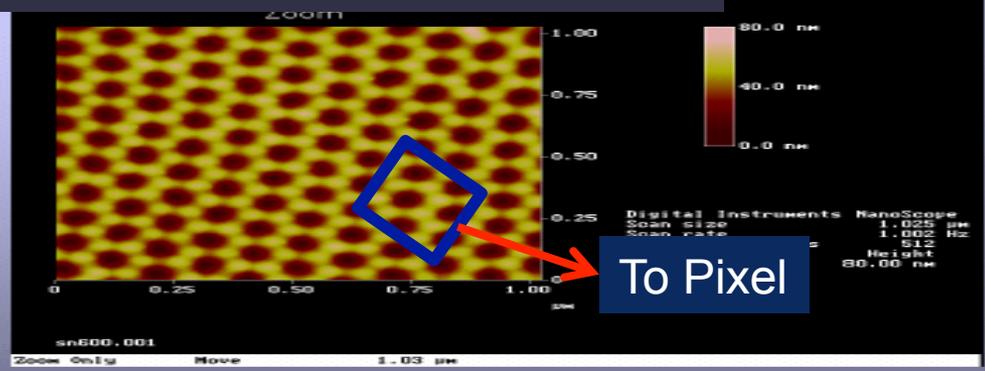
VCU

Circuit parameters based on measured values

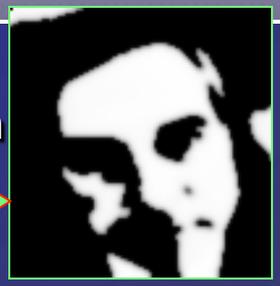


- Single dot : $R_{inter-dot} = 640 \text{ M}\Omega$
- Single dot : $C_{inter-dot} = 5 \text{ aF}$
- Single dot : $C_{substrate} = 0.5 \text{ aF}$
- Single dot : Peak current = 1.5 nA
- Superdot (1 pixel = 6400 dots): $R_{inter-superdot} = 8 \text{ M}\Omega$
- Superdot : $C_{inter-superdot} = 4 \text{ fF}$
- Superdot : $C_{substrate} = 3.2 \text{ fF}$
- Superdot : Peak current = 0.1 μA

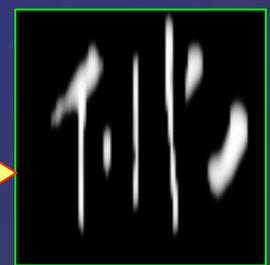
IEEE Trans. on Nanotech, 2008



Edge Detection

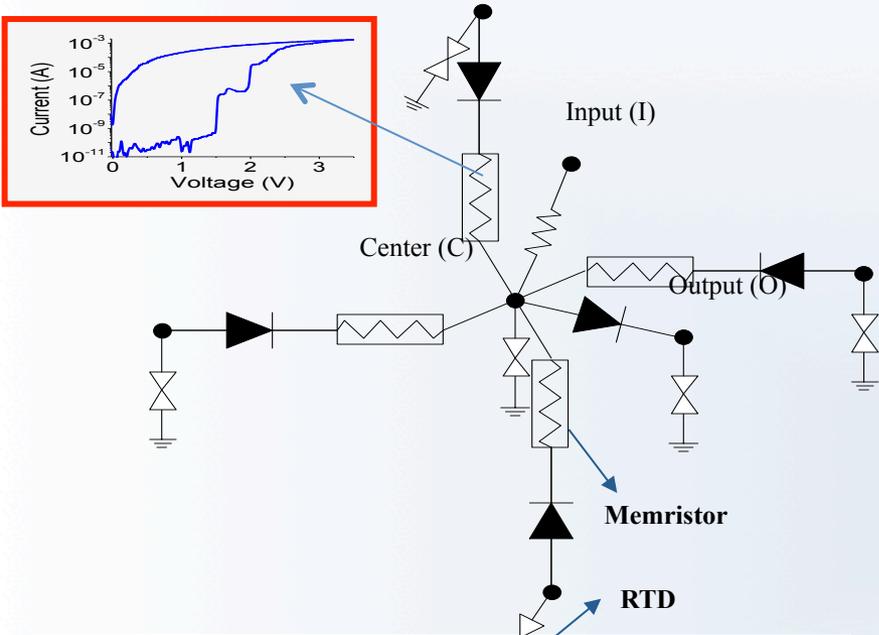


Vertical Line Detection

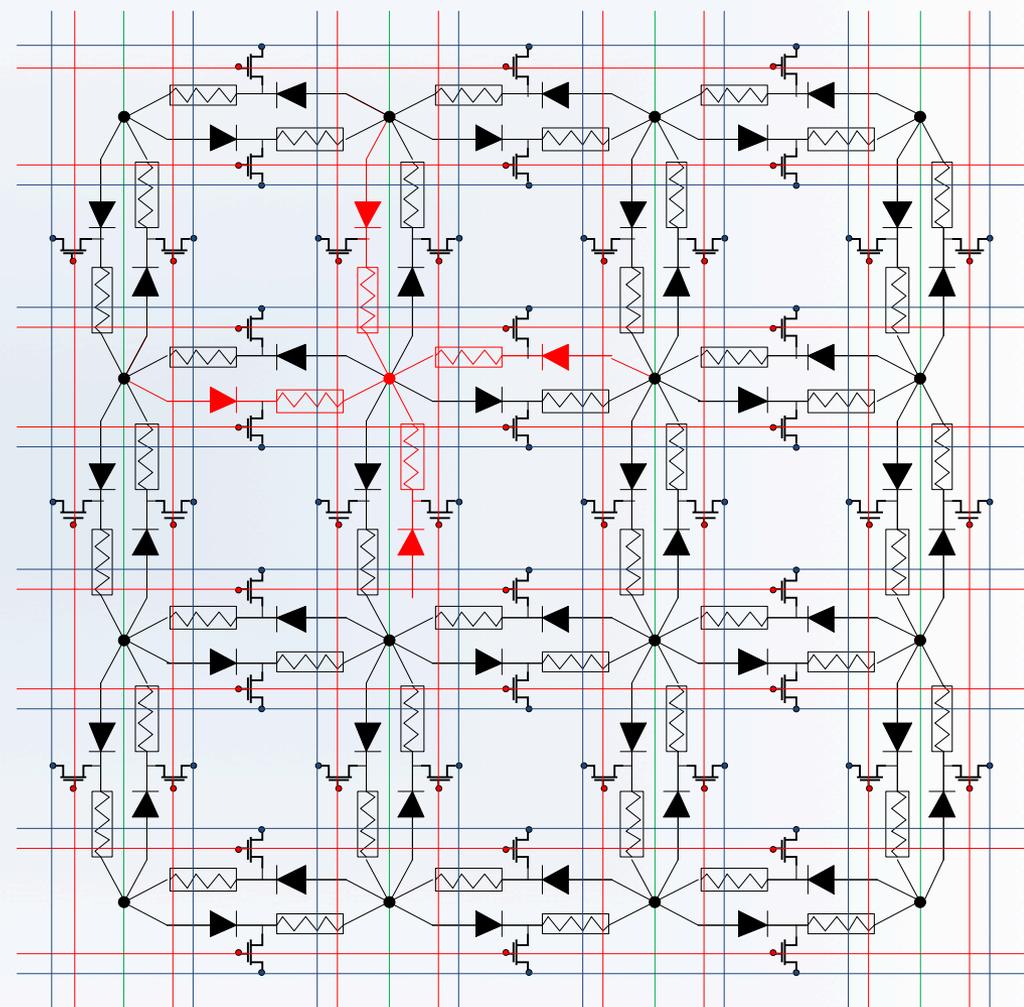
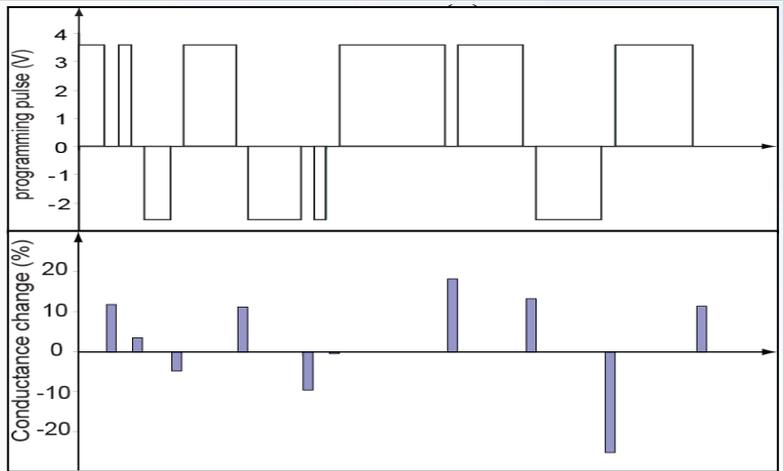


(C) 2015 Pro

Analog Programmable Nano-Architecture for Static and Dynamic Image Processing



IEEE Trans. On Nanotechnology, 2013

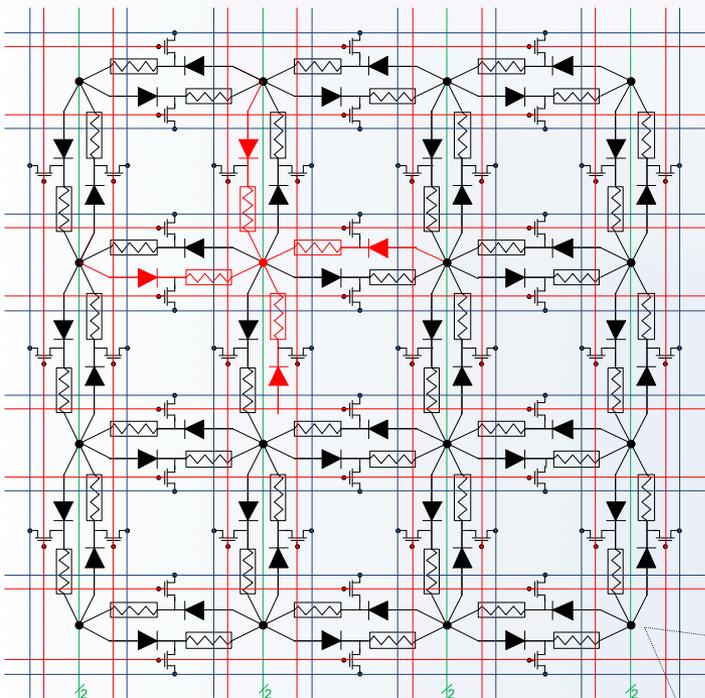


(b)

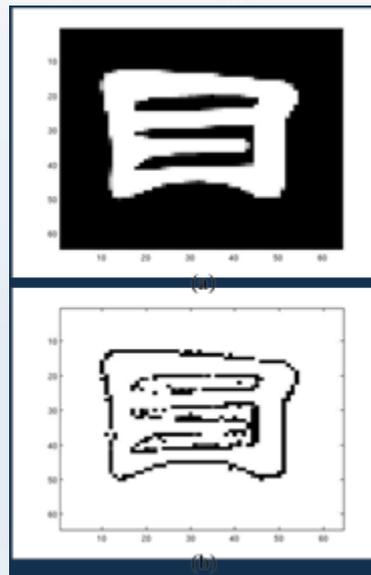
Qdot + Memristor Chip

Analog Programmable Unconventional Computing

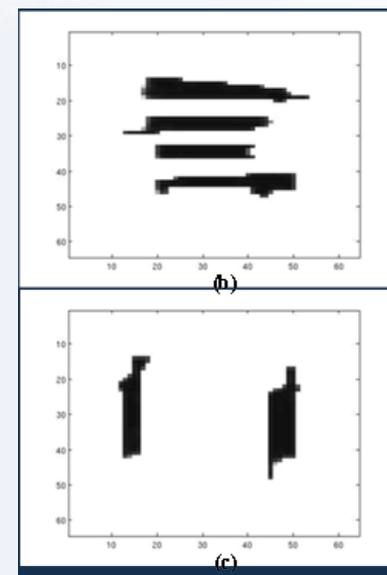
IEEE Trans. On Nanotechnology, 2013



Qdot + Memristor Chip



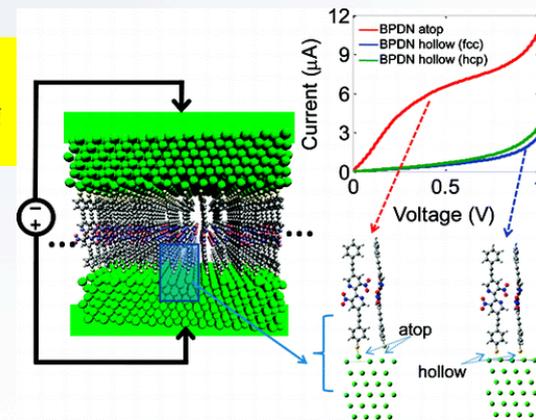
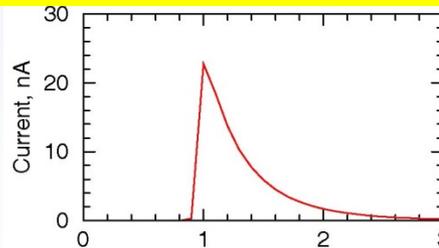
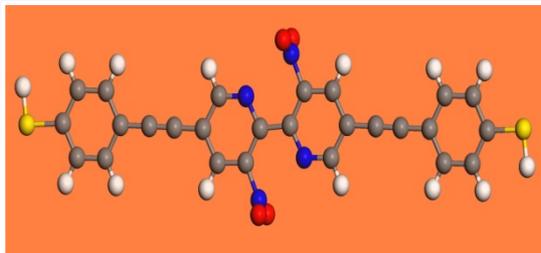
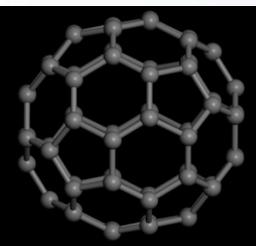
Edge Detection



HLD & VLD

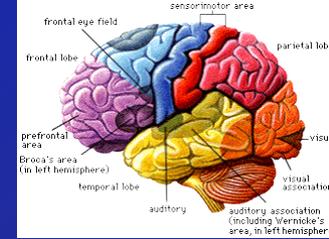
Molecular Computer?

$$H = \sum_i \varepsilon_0 (V_{tot}) c_i^+ c_i + hc_{i\pm 1}^+ c_i$$

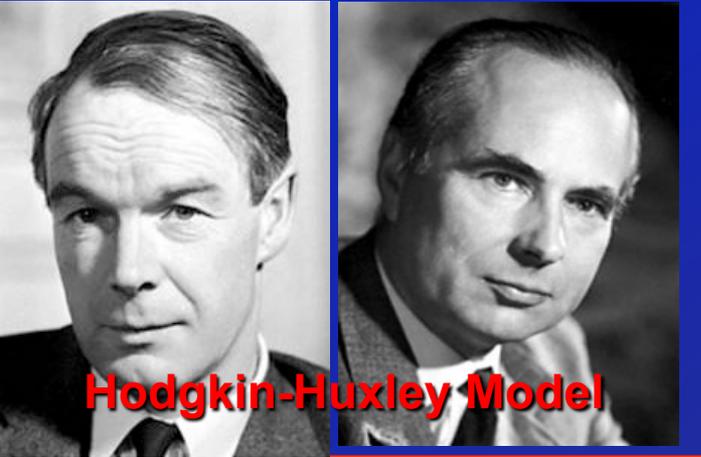


Spike Timing Dependent Plasticity (STDP) Learning Networks using Memristors

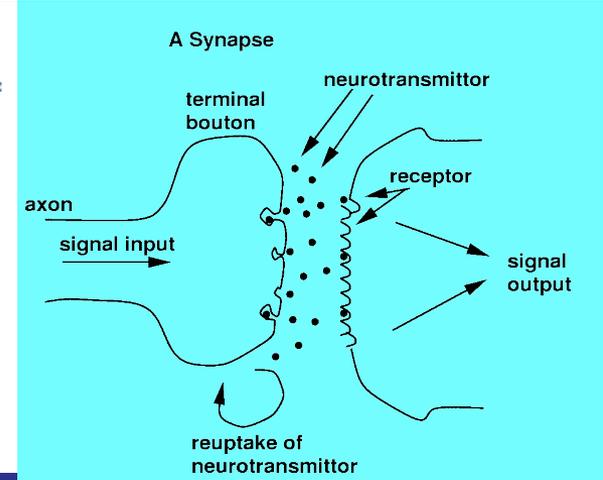
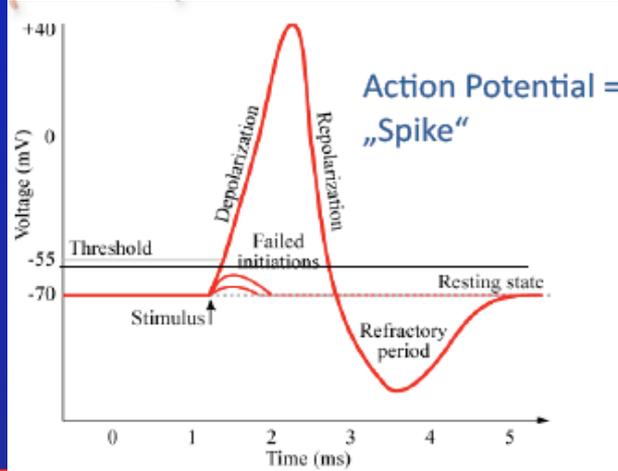
Biological Neuron Model



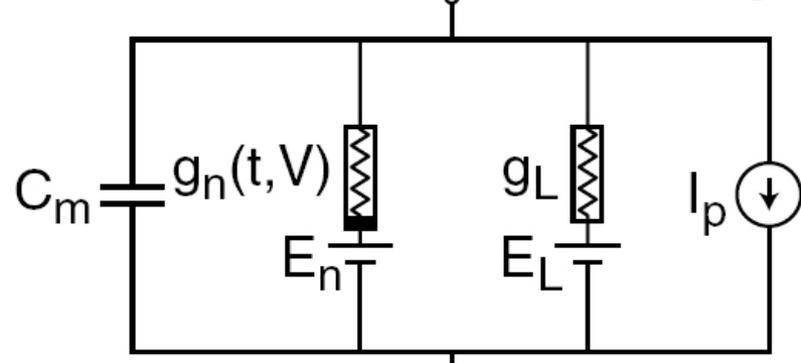
Ionic Transport in Biological Neuron & its Silicon Implementation



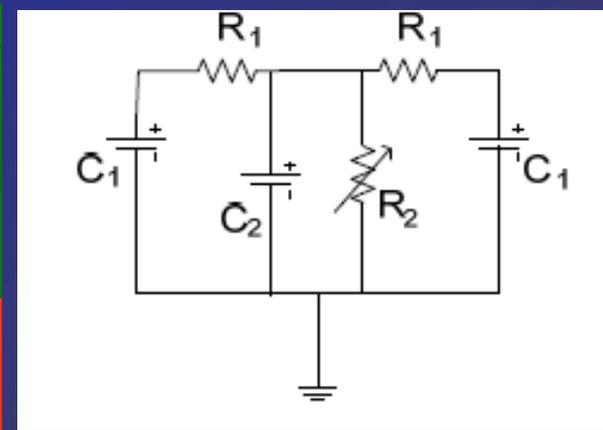
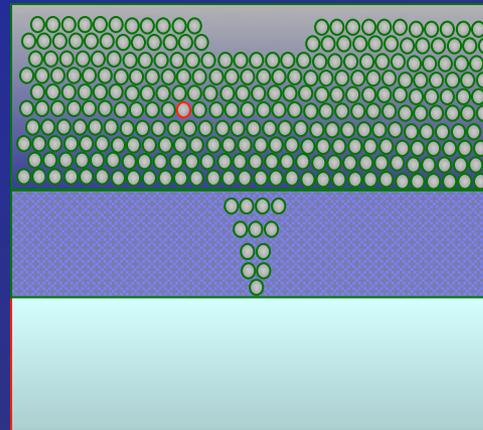
Hodgkin-Huxley Model



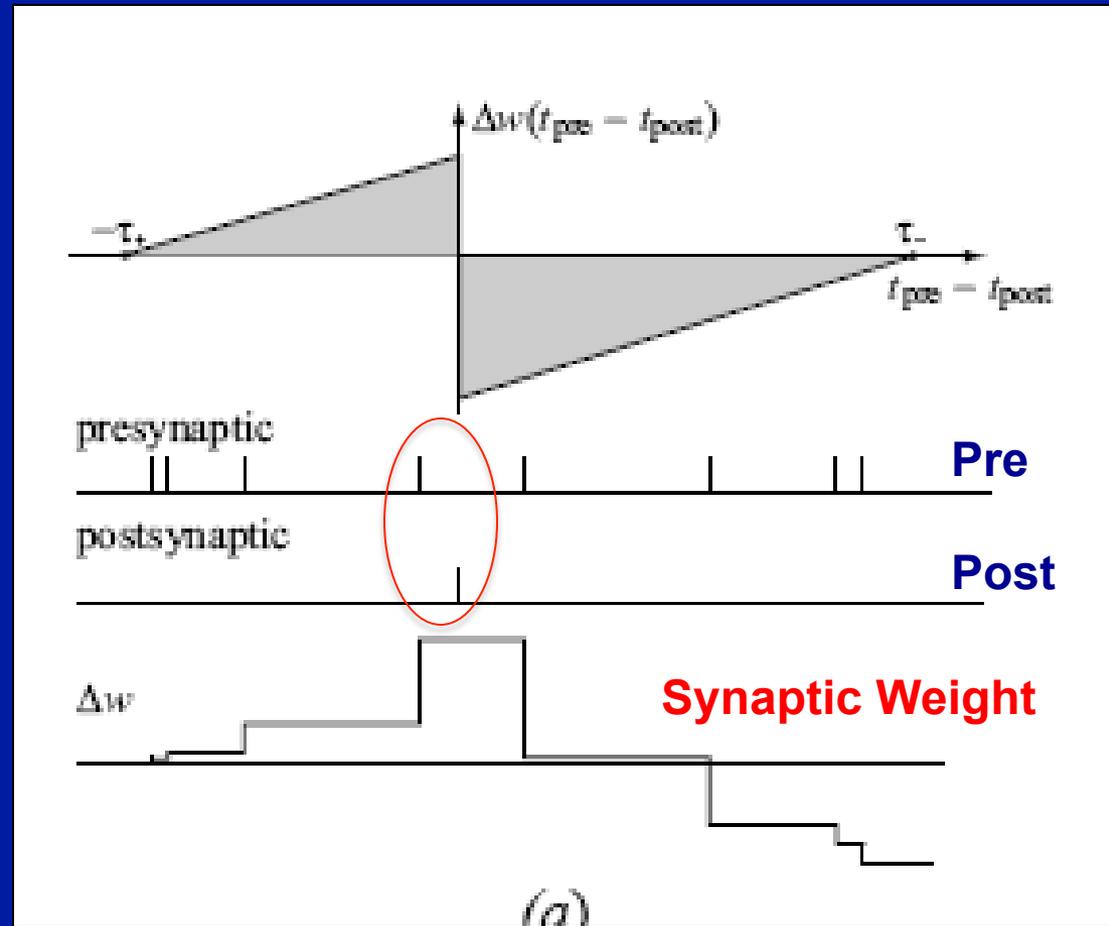
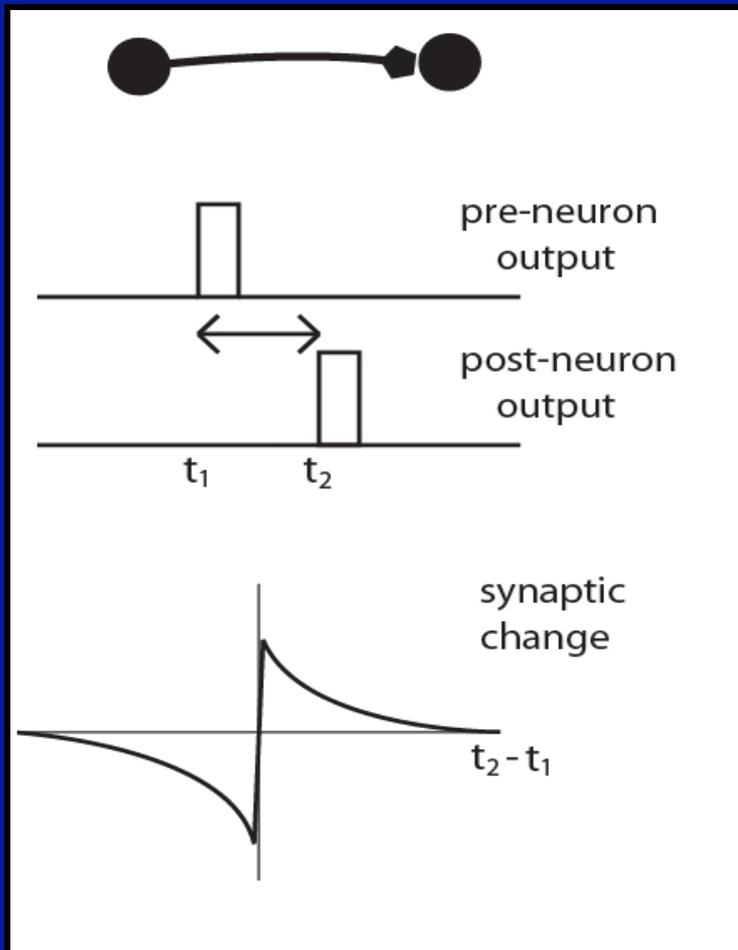
$$I(t, V) = g(t, V) \cdot (V - V_{eq})$$



$$C_m \frac{dV(t)}{dt} = - \sum_i I_i(t, V)$$

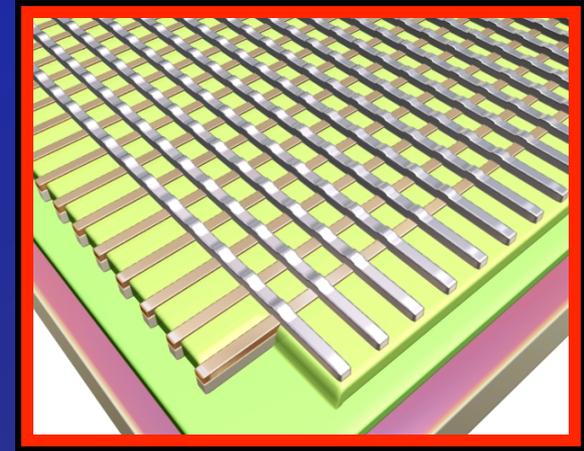
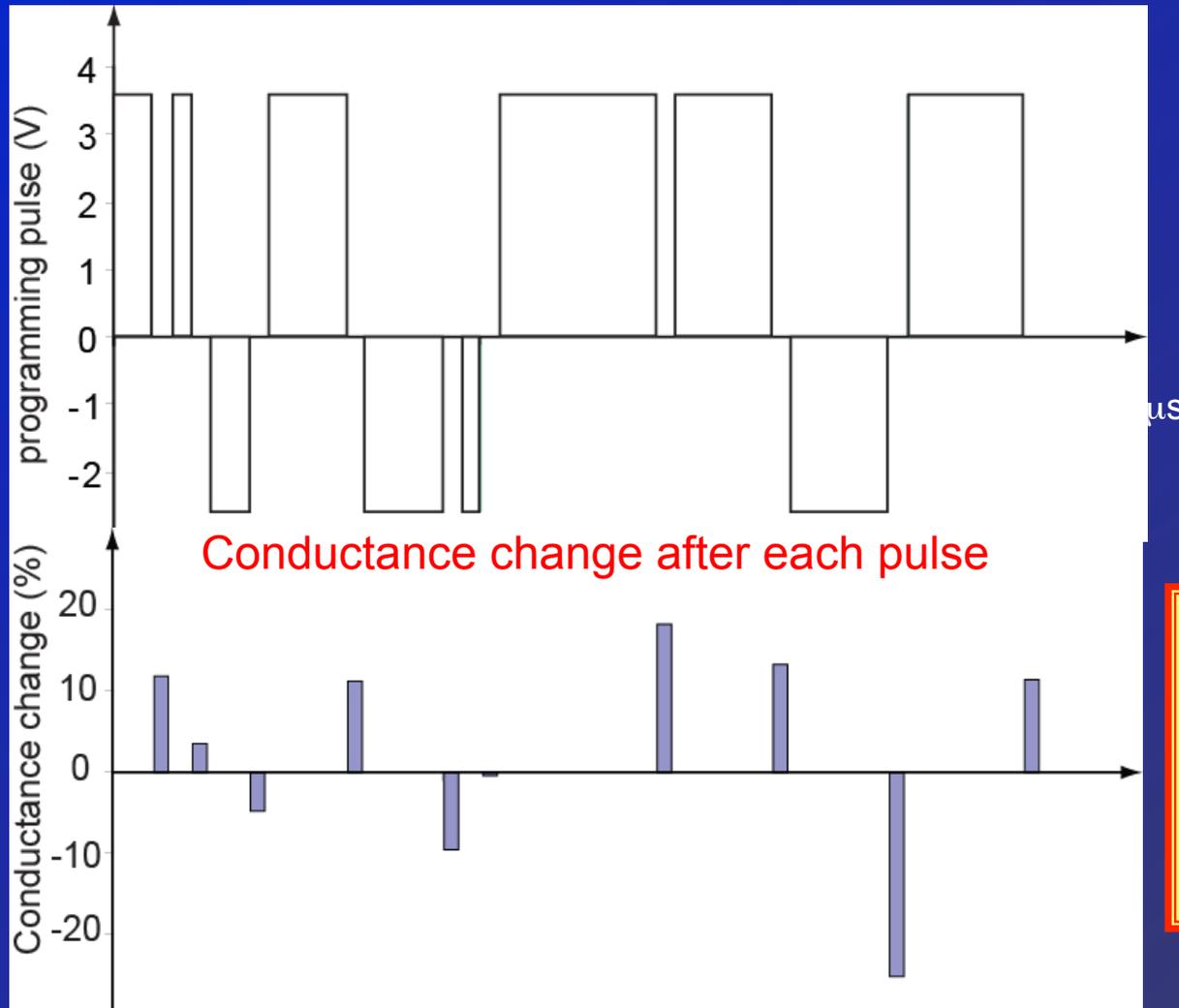


Spike Timing Dependent Plasticity (STDP) Learning Networks



Previous Approach of STDP Implementation On Crossbar with Constant Amplitude

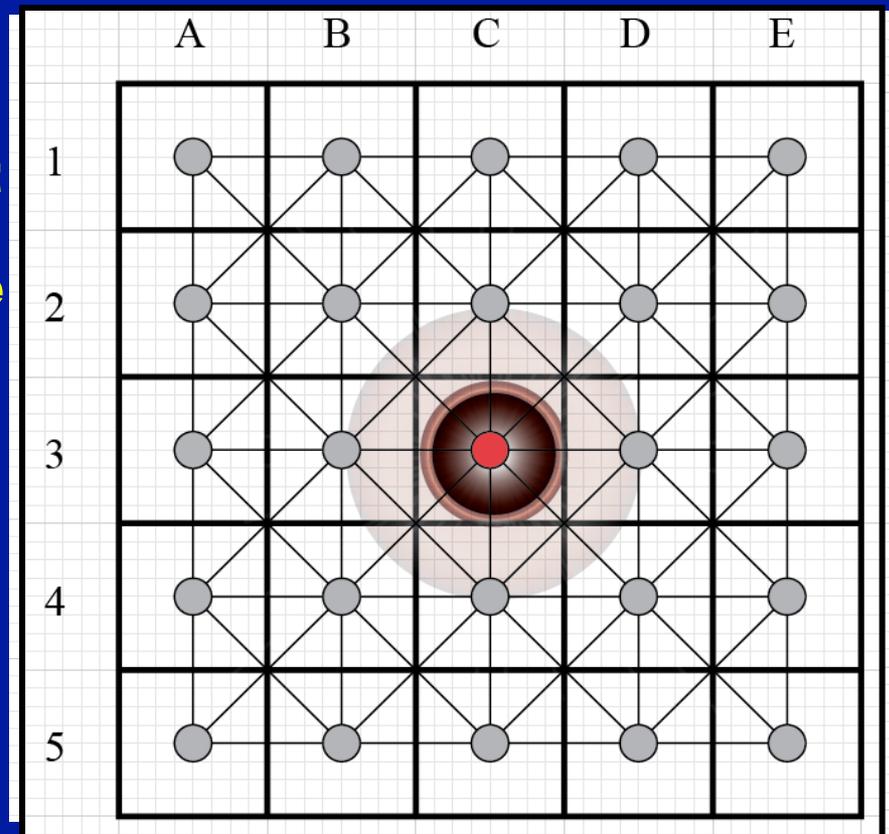
Programming pulses with different pulse widths



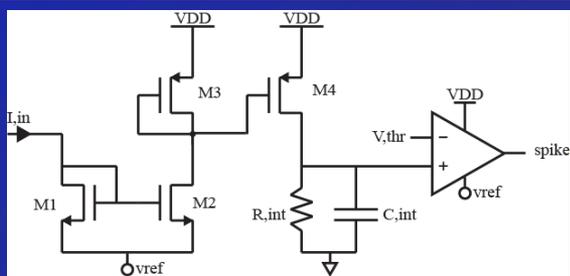
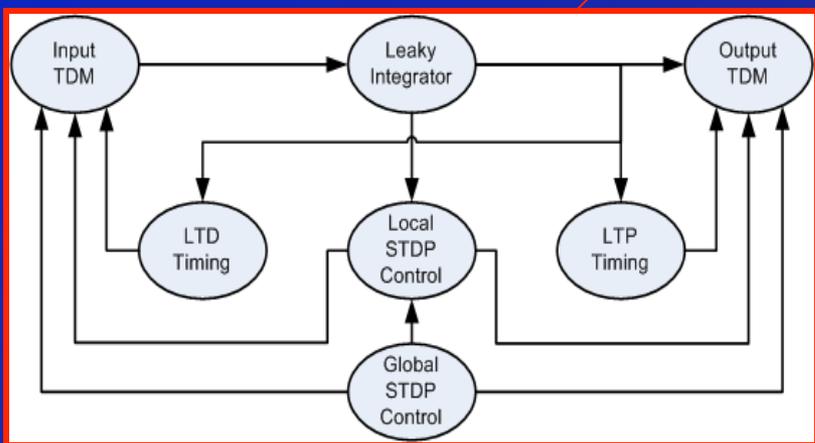
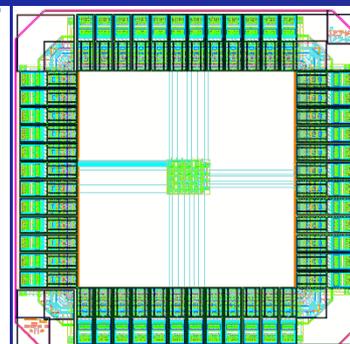
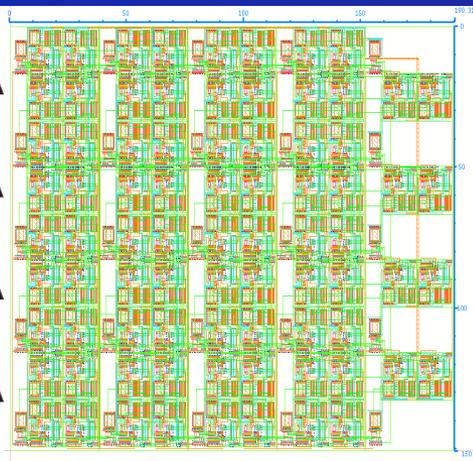
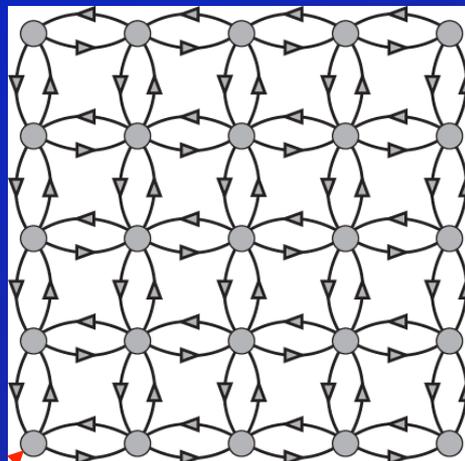
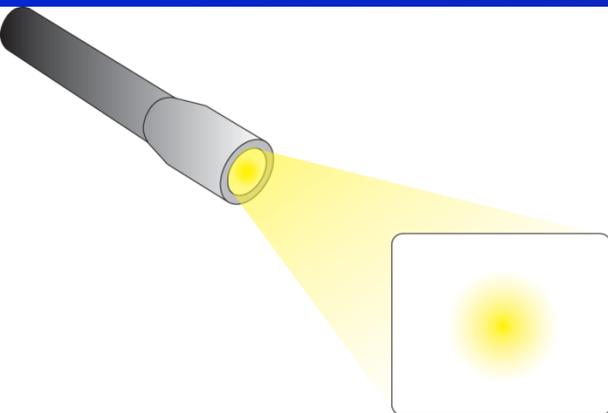
1. Digitally Controlled
2. Constant Amplitude
3. Temporal Correlation

Position Detector Application

- **Split up area into a 5x5 grid**
- **Each grid has one neuron that is connected to an adjacent neuron through STDP synapse**
- **Detect a light source at any position on the grid**
- **No post-processing circuitry necessary**
- **k-Winner-Take-All (k-WTA) implementation**

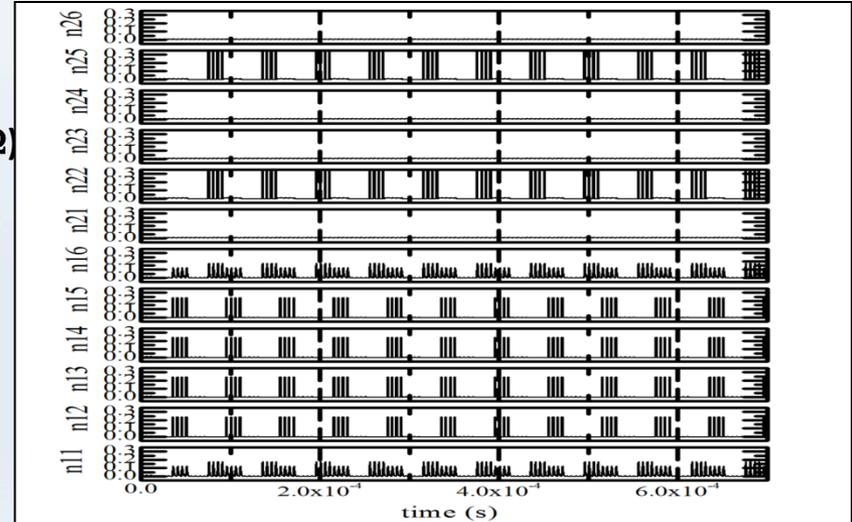
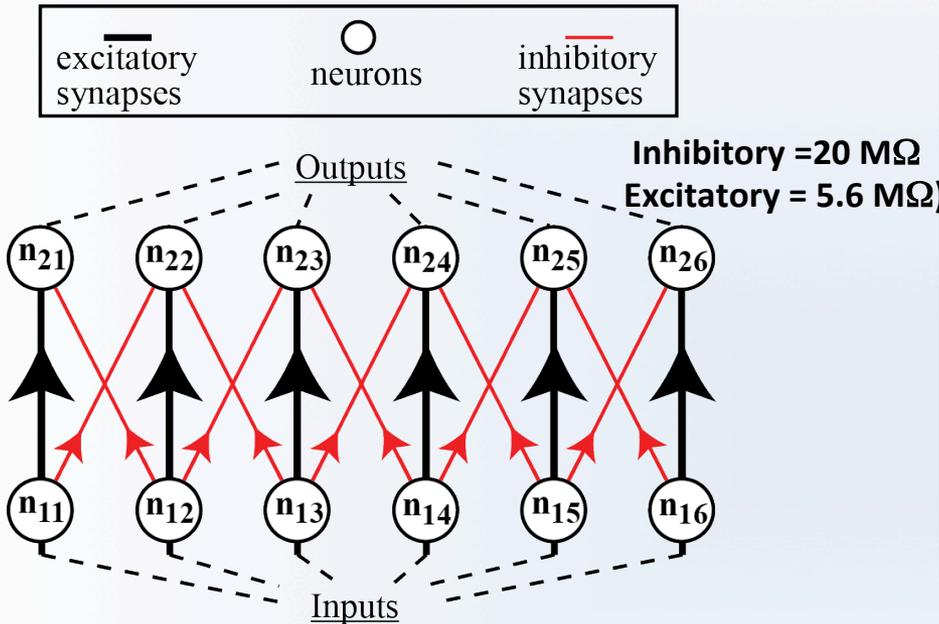


STDP Neural Circuit for Position Detector



Bases	Memristor Design	CMOS Design
Synaptic area	< (0.5 μm x 0.5 μm)	17 μm x 16 μm
Synaptic Density	\gg 4 devices/ μm^2 x1000	0.0037 devices/ μm^2
Neuron area	20 μm x 10 μm	8 μm x 12 μm
Neuron Density	0.005 devices/ μm^2 x2	0.0104 devices/ μm^2
Volatility	Nonvolatile	Volatile

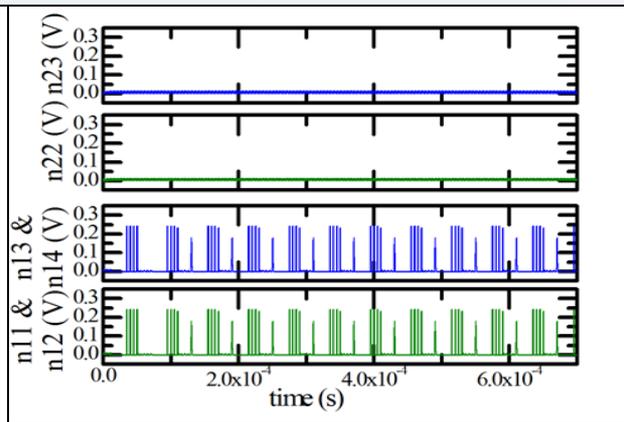
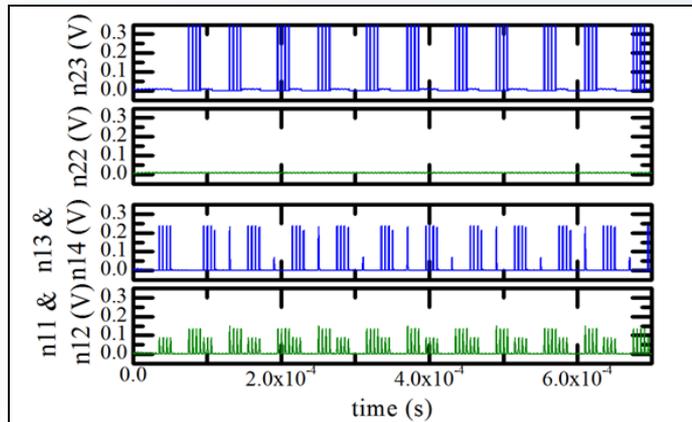
STDP Circuits for XOR/Edge Detector



Input = 011110; Output = 010010

$n_{23} = n_{12} \text{ XOR } n_{14} = 1$ when $n_{12}=0$ & $n_{14}=1$

$n_{23} = n_{12} \text{ XOR } n_{14} = 0$ when $n_{12}=1$ & $n_{14}=1$



Basic Neuromorphic Functions: WTA, XOR, Edge Detector Were implemented Using STDP learning scheme

IEEE Nano 2011

Reinforcement Learning Networks

Memristor Based
Q-Learning Network

CMOS Digital
Actor-Critic Network

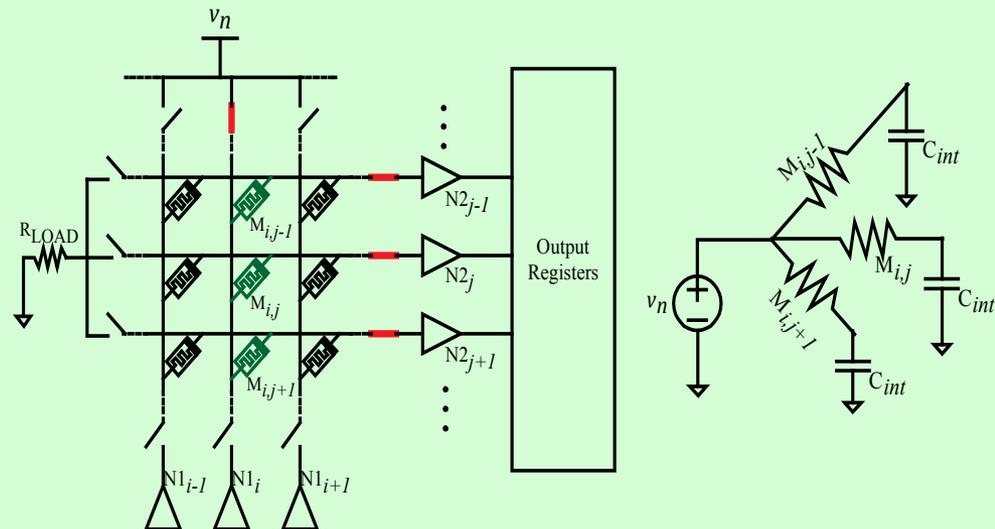
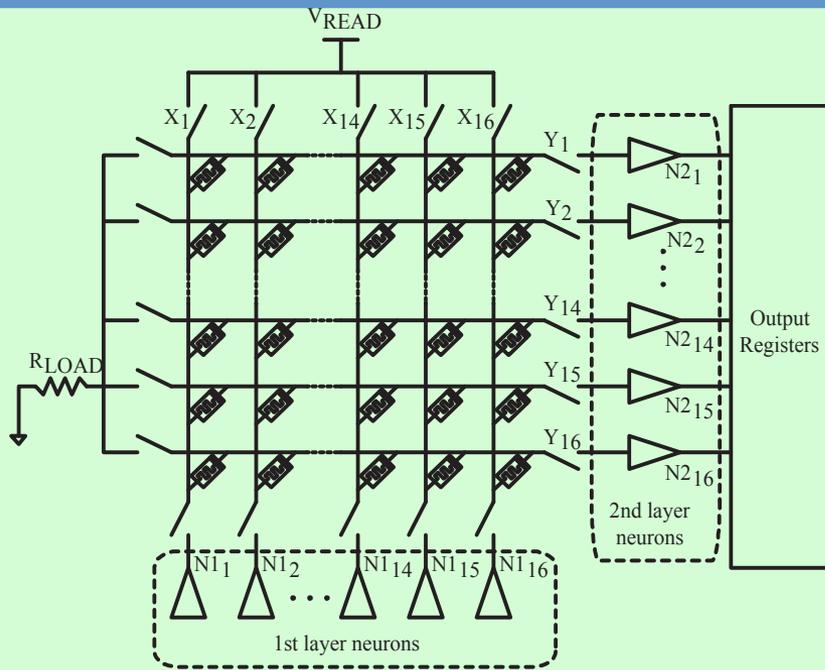
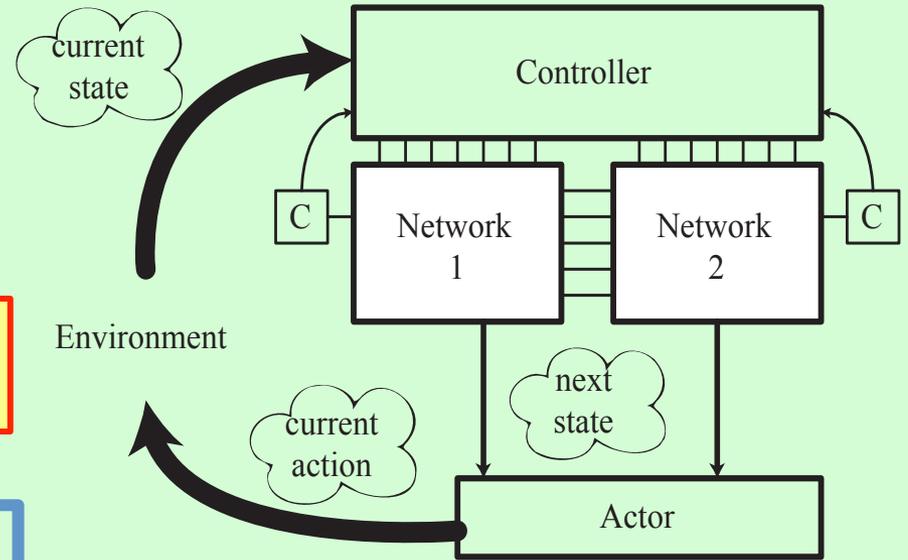
Q-Learning Hardware – Reinforcement Learning

$$\tilde{Q}(s_t, a_t) \leftarrow \tilde{Q}(s_t, a_t) \times (1 - \alpha_t(s_t, a_t)) + \alpha_t(s_t, a_t) \times r_t + \alpha_t(s_t, a_t) \times \max_{a_{t+1}} \left[\tilde{Q}(s_{t+1}, a_{t+1}) \right]$$

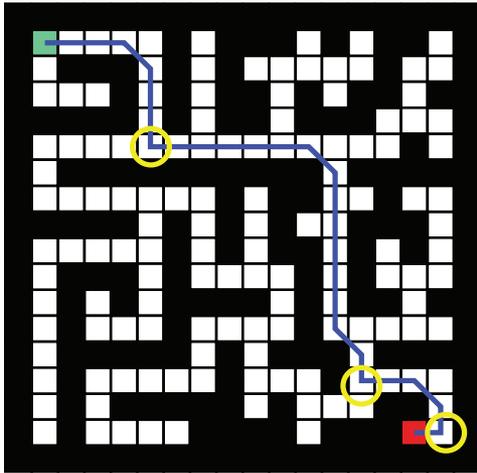
$$\max_{a_{t+1}} \left[\tilde{Q}(s_{t+1}, a_{t+1}) \right] = \tilde{Q}(s_t, a_t) + \delta_t.$$

$$\tilde{Q}(s_t, a_t) \leftarrow \tilde{Q}(s_t, a_t) + \alpha_t(s_t, a_t) \times (r_t + \delta_t)$$

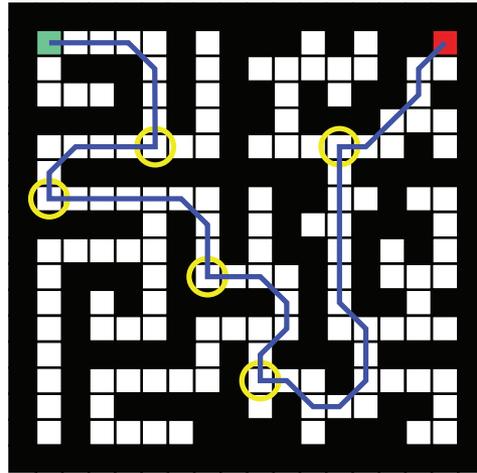
Evaluative Feedback (Rewards)



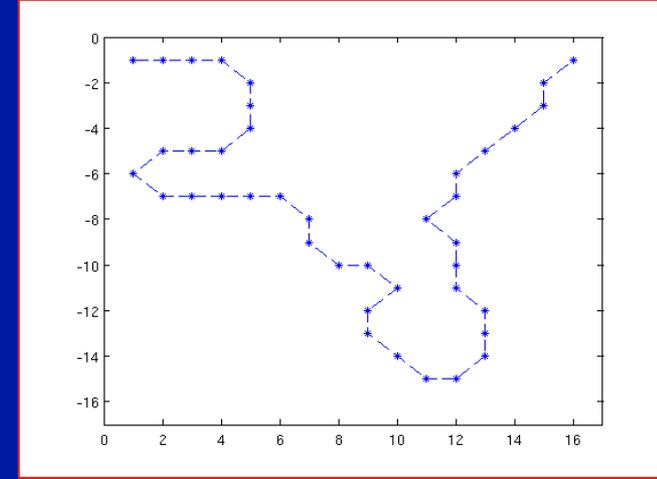
Performance of Memristor Q-Learning Hardware



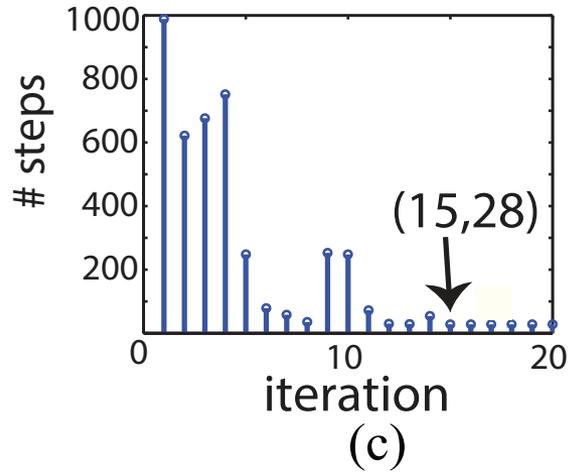
(a)



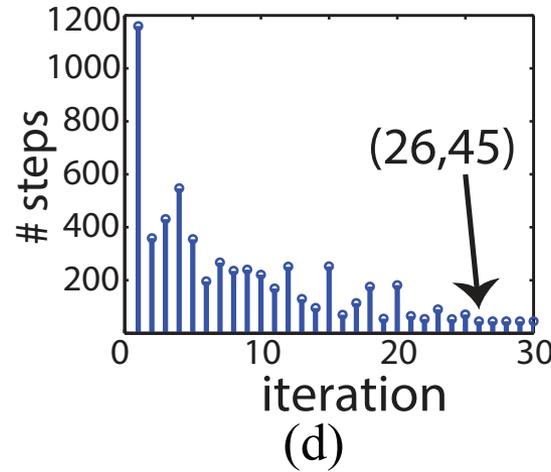
(b)



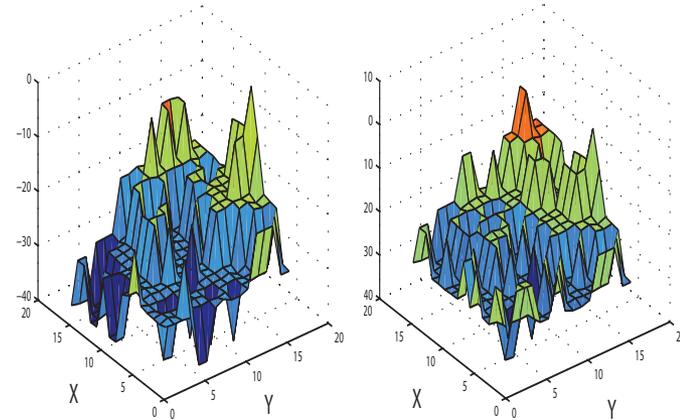
Memristor Model Used in Matlab Simulation



(c)



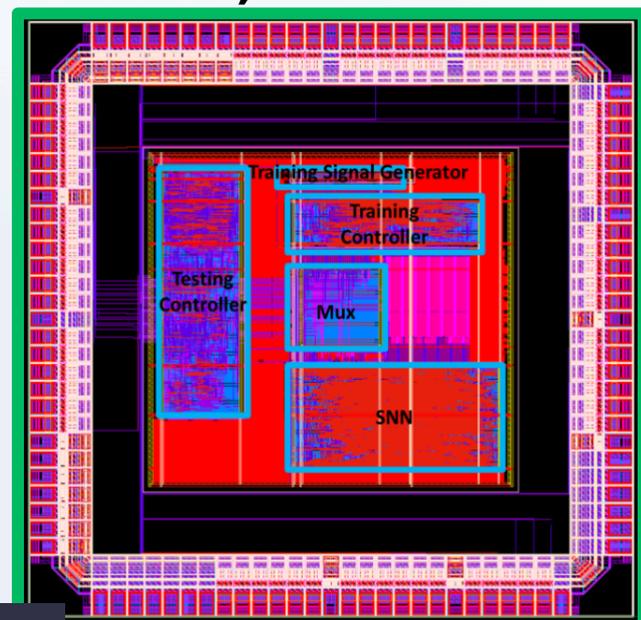
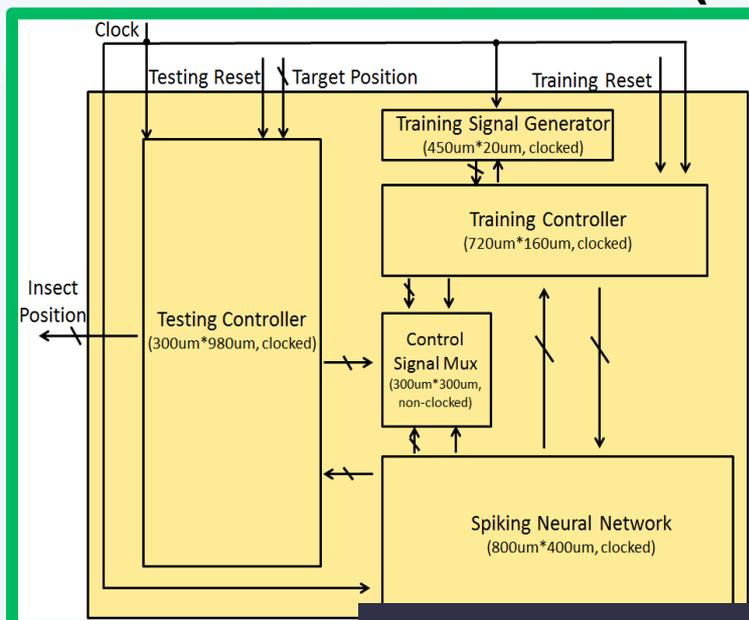
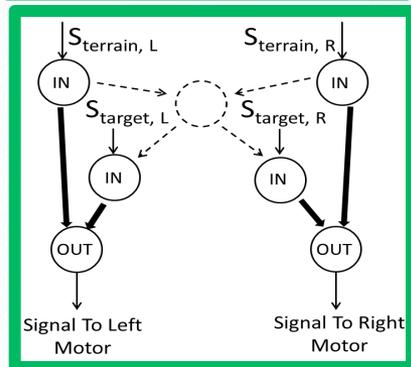
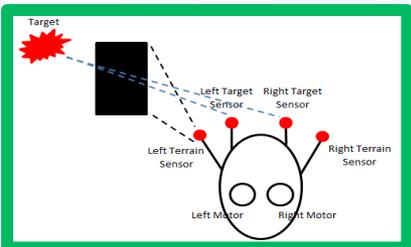
(d)



Synapse States after 1st and 2nd Iterations

Plasticity (STDP) Based Learning Chip for Virtual Bug Navigation

Non-Evaluative Feedback (Correlation)



VLSI Journal, 2015

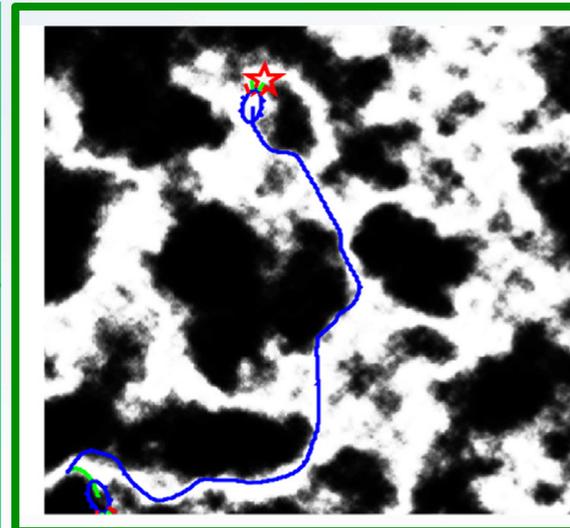
$$\begin{cases} V_x = V^* \cdot \cos(\theta) \\ V_y = V^* \cdot \sin(\theta) \\ V = \frac{V_L + V_R}{2} \\ \Delta\theta = \frac{V_R - V_L}{L} \\ \Delta V_L = -\frac{V_L}{\tau_{motor}} + \eta * (t == t_L^f) \\ \Delta V_R = -\frac{V_R}{\tau_{motor}} + \eta * (t == t_R^f) \end{cases}$$

$$\Delta w_{ij}^r = \begin{cases} A_+ \cdot e^{-\frac{D_{ij}^r}{\tau_+}}, & D_{ij}^r > 0 \\ -A_- \cdot e^{-\frac{D_{ij}^r}{\tau_-}}, & D_{ij}^r < 0 \end{cases}$$

$$D_{ji}^{r+1} = D_{ji}^r - \alpha \frac{\partial e}{\partial w_{ij}^r} \quad D_{ij}^r > 0$$

$$D_{ji}^{r+1} = D_{ji}^r - \alpha \frac{\partial e}{\partial w_{ij}^r} \quad D_{ij}^r < 0$$

$$D_{ji}^r = T_j^r - T_i^r \quad D_{ji}^{r+1} = D_{ji}^r - \alpha \frac{\partial e}{\partial w_{ji}^r}$$

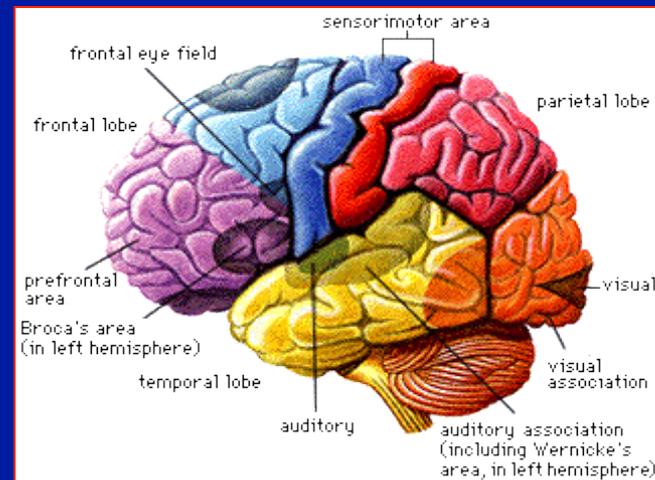
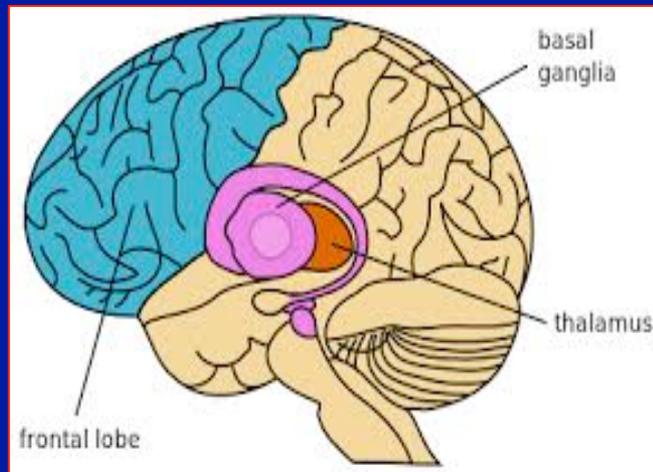


Conclusion

Facets of Neuromorphic or Brain-like Computing:

1. Self-Healing
3. Cognition

2. Learning & Plasticity
3. Associative Memory



Adaptive Hardware Platform: Optimal control theory, multi-agent systems, swarm intelligence, robot control, computer games, telecommunications, smart grid for power distribution, and Markov decision process (MDP)